Electronic Version
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Description

NON-VOLATILE MEMORY AND METHOD OF OPERATION

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention provides a non-volatile memory and a method of programming and erasing, and more particularly, the present invention relates to an electrically erasable programmable read-only memory (EEPROM) and a method of programming and erasing.

[0003] 2. Description of the Prior Art

[0004] An EEPROM device is a kind of non-volatile memory. The structure of EEPROMs is similar to that of erasable programmable read-only memories (EPROMs) since both of them have a floating gate for storing charges and a control gate for controlling data access. In a large number of memory cells, each memory cell comprises a floating gate for storing charges which represent data. After the float-

ing gate of the memory cell is charged, the threshold voltage of the memory cell is lifted, so the charged memory cell will not be in a conductive state during addressing in reading. A state of not conducting is regarded as a "0" state or a"1" state by detecting circuits utilizing a binary system. Uncharged memory cells will be regarded as being in a "1" state or in a "0"state correspondingly. In comparison with an EPROM which is programmed and erased as a whole, EEPROM has the advantage of erasing and programming data bit by bit. Therefore, the EEPROM is a byte addressable device.

[0005] Since the flash memory is erased block by block rather than bit by bit, EEPROM is superior to the flash memory in partial data revision when compared with the flash memory product, which is rapidly growing in market. The EEPROM is very suitable to be used in an embedded function, such as an address book in cell phones, because of its byte program/erase feature. In addition, EEPROM products usually have good high reliability performance, which increases applicability in application fields requiring repetitive programming, reading, and erasing.

[0006] Please refer to Fig.1, Fig.1 is a cross-sectional schematic diagram illustrating a prior art EEPROM device 10. As

shown in Fig.1, the prior art EEPROM device 10 is disposed on a semiconductor wafer 11. The semiconductor wafer 11 comprises a P-type silicon substrate 12. The EEPROM device 10 comprises a memory cell 14. The memory cell 14 comprises a source region 16 and a drain region 18 disposed on a surface of the P-type silicon substrate 12, and a channel region 22 between the source region 16 and the drain region 18. Both the source region 16 and the drain region 18 are N-type heavy doped regions. The memory cell 14 further comprises a tunnel oxide layer 24, a floating gate 26, a dielectric layer 28, and a control gate 32. The tunnel oxide layer 24 is disposed on a top surface 25 of the P-type silicon substrate 12, and the tunnel oxide layer 24 covers the channel region 22. The floating gate 26 is disposed on a surface of the tunnel oxide layer 24. The dielectric layer 28 covers the floating gate 26. The control gate 32 is disposed on a surface of the dielectric layer 28 and the surface of the tunnel oxide layer 24.

[0007] The EEPROM device 10 further comprises an N-type select gate transistor 34. The select gate transistor 34 comprises a source region 36, a drain region, and a gate 38. Since the drain region of the N-type select gate transistor 34 is

overlapped with the source region 16 of the memory cell 14, it is not specially marked. In addition, the source region 36 of the N-type select gate transistor 34 is electrically connected to a bit line (BL).

[0008] When the memory cell 14 is selected to perform a program operation, a high positive potential (such as +12V) is supplied to the control gate 32. At this time, the N-type select gate transistor 34 is turned on to pass a program potential (such as 2.5V) supplied to the bit line to the source region 16 of the memory cell 14. In addition, a terminal 42 electrically connected to the P-type silicon substrate 12 is grounded. Since the program potential and the potential of the P-type silicon substrate 12 are obviously lower than the positive potential supplied to the control gate 32, high potential differences exist to produce an electric field that transverses the tunnel oxide layer 24. Therefore, electrons flowing from the source region 16 to the drain region 18 will acquire kinetic energy due to the existence of the electric field, and change their acceleration direction and transverse the tunnel oxide layer 24 by Fowler-Nordheim (FN) tunneling mechanism. The electrons then are injected into the floating gate 26 and are trapped in the floating gate 26 to complete the

program operation. The threshold voltage of the N-type memory cell 14 is thus lifted.

[0009] When the memory cell 14 is selected to perform an erase operation, a high negative potential (such as -12V) is supplied to the control gate 32. At this time, the N-type select gate transistor 34 is turned on to pass an erase potential (such as +2.5V) supplied to the bit line to the source region 16 of the memory cell 14. In addition, the terminal 42 electrically connected to the P-type silicon substrate 12 is grounded. Since the erase potential and the potential of the P-type silicon substrate 12 are obviously higher than the potential supplied to the control gate 32, not only is the channel region 22 of the memory cell 14 not conducted, but also high potential differences exist to produce an electric field that transverses the tunnel oxide layer 24 (opposite to the direction of the electric field when programming). Therefore, electrons stored in the floating gate 26 will be driven to move toward the channel region 22, and are sucked out to the channel region 22 from the floating gate 26 by Fowler-Nordheim tunneling mechanism. The erase operation is thus completed.

[0010] In the prior art, both the program operation and the erase

operation which charge or discharge the floating gate utilizes Fowler-Nordheim tunneling mechanism. This method has its native limitation in that the Fowler-Nordheim tunneling behavior of electrons does not happen under the electric field produced by a low potential difference. That means, in order to make this behavior happen, a high potential difference must exist to result in a very slow program speed and erase speed. Furthermore, electrons enter and leave the floating gate 26 through a tunnel window 44, as shown in Fig.1, in the prior art. Because the tunnel oxide layer 24 inside the tunnel window 44 is very thin, the tunneling behavior of electrons is benefited to improve the performance of the memory device. However, a process problem is encountered.

[0011] In the prior art memory cell 14, a buried implant region 46 is respectively formed in portions of the channel region 22 near the source region 16 and the drain region 18, as shown in Fig.1, before forming the tunnel window 44. The buried implant region 46 is an N-type lightly doped region. The objective of forming the buried implant regions 46 is to lift tunneling efficiency so as to improve program speed and hot electrons injection. Since the tunnel window 44 is within the range of the buried implant region

46, it thus becomes very difficult when aligning the tunnel window 44. In consideration of this problem, the size of the tunnel window 44 cannot be shrunk to avoid the mis-alignment problem, leading to a barrier to memory cell 14 shrinkage. In some of the prior arts, the methods for forming tiny tunnel windows are taught. However, process steps are complex in these methods to increase processing complexity and cost of products.

[0012] Therefore, it is very important to develop a new EEPROM structure. This EEPROM structure should perform program and erase under low operation voltages to improve operation speed. In addition, the need of the tunnel window is eliminated in this EEPROM structure such that the memory cell is shrunk without increasing processing complexity and product costs.

SUMMARY OF INVENTION

[0013] It is therefore a primary objective of the present invention to provide an EEPROM structure and a method of programming and erasing to resolve the above-mentioned problems.

[0014] The present invention provides a method of programming and erasing an EEPROM device. The method comprises performing a band-to-band tunneling induced hot-

electrons program via a program bit-line and performing a Fowler-Nordheim tunneling erase via an erase bit-line. The EEPEOM device comprises a P-type transisitor, an N-type transistor, and a double gate P-type transistor. A source of the P-type transistor is electrically connected to the program bit-line. A source of the N-type transistor is electrically connected to the erase bit-line. A drain of the double gate P-type transistor is electrically connected to a drain of the P-type transistor and a drain of the N-type transistor.

[0015] It is an advantage of the present invention that the present invention EEPROM device utilizes the P-type EEPROM cell to replace the N-type EEPROM cell. Furthermore, a P-type select gate transistor electrically connected to the program bit-line is utilized to perform the band-to-band tunneling induced hot-electrons program, and an N-type select gate transistor electrically connected to the erase bit-line is utilized to perform the Fowler-Nordheim tunneling erase. Owing to the considerable current generated by the band-to-band tunneling induced hot-electrons phenomenon, the injection of hot electrons caused by band-to-band tunneling mechanism is faster than that caused by Fowler-Nordheim tunneling mecha-

nism. Therefore, program speed is greatly improved. Because of the obviously lifted program efficiency, the tunnel window, adapted in the prior art EEPROM device structure, can be replaced by a common tunnel oxide layer in the present invention EEPROM device structure. As a result, the problems of complex processing and raised cost incurred from misalignment, which usually occurs in the prior art, are avoided. The barrier to device shrinkage is not encountered. In addition, operation voltage is obviously lowered to expand the range of application under the industry stream of lightweight and small size.

[0016] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0017] Fig.1 is a cross-sectional schematic diagram illustrating a prior art EEPROM device.

[0018] Fig.2 is a layout diagram of the present invention EEPROM device.

[0019] Fig.3 is a cross-sectional schematic diagram of the EEPROM device shown in Fig.2.

[0020] Fig.4 is a cross-sectional schematic diagram along line 4-4" of the EEPROM device shown in Fig.2.

[0021] Fig.5 is a circuit diagram of the present invention EEPROM device.

[0022] Fig.6 is an example table illustrating operation voltages of the present invention EEPROM device.

DETAILED DESCRIPTION

[0023] Please refer to Fig.2 to Fig.4, Fig.2 is a layout diagram of the present invention EEPROM device 100. Fig.3 is a cross-sectional schematic diagram of the EEPROM device 100 shown in Fig.2. Fig.4 is a cross-sectional schematic diagram along line 4-4" of the EEPROM device 100 shown in Fig.2. As shown in Fig.2 and Fig.3, the present invention EEPROM device 100 is disposed on a semiconductor wafer 101. The semiconductor wafer 101 comprises a P-type silicon substrate 102, a deep N-well (DNW) 103 disposed in the P-type silicon substrate 102, and a P-well (PW) 104 disposed in the deep N-well 103. The EEPROM device 100 comprises a P-type memory cell 106, an N-type select gate transistor 108, and a P-type select gate transistor 112.

[0024] The memory cell 106 comprises a source region 114 and a drain region 116 disposed on a surface of the deep N-

well 103, and a channel region 118 between the source region 114 and the drain region 116. Both the source region 114 and the drain region 116 are P-type heavy doped regions, and the source region 114 is electrically connected to a source line (SL). The memory cell 106 further comprises a tunnel oxide layer 122, a floating gate 124, a dielectric layer 126, and a control gate 128. The tunnel oxide layer 122 is disposed on a top surface 123 of the deep N-well 103, and the tunnel oxide layer 122 covers the channel region 118. The floating gate 124 is disposed on a surface of the tunnel oxide layer 122. The dielectric layer 126 covers the floating gate 124. The control gate 128 is disposed on a surface of the dielectric layer 126 and the surface of the tunnel oxide layer 122.

[0025] The N-type select gate transistor 108 comprises a source region 132, a drain region 134, and a select gate (SG)136. The source region 132 of the N-type select gate transistor 108 is electrically connected to an erase bit line (Eb1). The P-type select gate transistor 112 comprises a source region 138, a drain region, and a select gate 142. Since the drain region of the P-type select gate transistor 112 is overlapped with the drain region 116 of the memory cell 106, it is not specially marked. The source region 138 of

the P-type select gate transistor 112 is electrically connected to a program bit line (Pb1). Because the select gates 136, 142 and the floating gate 124 in the memory cell106 are formed by etching a same polysilicon layer, a polysilicon layer 143 is shown on top of each of the select gates 136, 142 in Fig.3.

[0026] When viewing along line 4-4", the deep N-well 103 is disposed in the P-type silicon substrate 102, and the P-well 104 is disposed in the deep N-well 103. The tunnel oxide layer 122 is disposed on the P-type silicon substrate 102. A polysilicon layer 125 used as the floating gate 124 is disposed on the tunnel oxide layer 122. The dielectric layer 126 covers the polysilicon layer 125 used as the floating gate 124. Another polysilicon layer 129 used as the control gate 128 is disposed on the dielectric layer 126 and the tunnel oxide layer 122, as shown in Fig.4. In addition, the P-well 104 and the deep N-well 103 are isolated from each other by a shallow trench isolation 144.

[0027] By cross-referring Fig.2, Fig.3, and Fig.4, it is very clear to see the polysilicon layers 146 disposed in pairs and in parallel, the heavy doped region used as the source region 132 of the N-type select gate transistor 108 disposed in the P-well 104, the heavy doped region used as the

source region 138 of the P-type select gate transistor 112 disposed in the deep N-well 103, and the shallow trench isolations 144 used for isolating the P-well 104 and the deep N-well 103 in Fig.2. It is worth noting that the shallow trench isolations 144 are not shown in Fig.3 in order to prepare the drawing more conveniently.

[0028] Please refer to Fig.5, Fig.5 is a circuit diagram of the present invention EEPROM device 100. As shown in Fig.5, the present invention EEPROM device 100 comprises the P-type select gate transistor 112, the N-type select gate transistor 108, and the P-type memory cell 106. The source region 138 of the P-type select gate transistor 138 is electrically connected to the program bit-line, and the source region 132 of the N-type select gate transistor 108 is electrically connected to the erase bit-line. The drain region 116 of the P-type memory cell 106 is electrically connected to the drain of the P-type select gate transistor 112 (overlapping with the drain region 116 of the memory cell 106) and the drain region 134 of the N-type select gate transistor. The P-type select gate transistor 112 and the N-type select gate transistor 108 are electrically connected through the select gates 136, 142 (please refer to Fig.3), and the P-type memory cell 106 is simultaneously

electrically connected to the P-type select gate transistor 112 and the N-type select gate transistor 108 due to the special layout shown in Fig.2.

[0029] Please refer to Fig.6, Fig.6 is an example table illustrating operation voltages of the present invention EEPROM device 100. As shown from Fig.3 to Fig.6, a first positive potential (such as +8V) is supplied to the control gate 128 such that the positive voltage is capacitively coupled to the floating gate 124 to build an electric field that transverses the tunnel oxide layer 122, when the present invention EEPROM device 100 performs programming. Then a negative potential (such as 8V) is supplied to the select gate 142 of the P-type select gate transistor 112 to turn on the P-type select gate transistor 112. When a negative program potential (such as 6V) is supplied to the program bit-line, the program potential is therefore passed to the drain region 116 of the P-type memory cell 106 through the turned-on P-type select gate transistor 112. Since a high positive potential difference exists between the control gate 128 and the drain region 116, band-to-band tunneling (BTBT) phenomenon thus occurs to generate electron-hole pairs at a junction of the drain region 116 of the P-type memory cell 106. Electrons in the electron-

hole pairs are accelerated by the electric field in the depletion region to acquire sufficient energy to become hot electrons. The hot electrons then inject into the floating gate 124 to complete the band-to-band tunneling induced hot-electrons (BTBTIHE) program.

[0030] When the present invention EEPROM device 100 performs erasing, a second negative potential (such as 8V) is supplied to the control gate 128 first. Then a second positive potential (such as +10V) is supplied to the select gate 136 of the N-type select gate transistor 108 to turn on the N-type select gate transistor 108. When a positive erase potential (such as +8V) is supplied to the erase bit-line, the erase potential is passed to the drain region 116 of the P-type memory cell 106 through the turned on N-type select gate transistor 108. Since a high negative potential difference exists between the control gate 128 and the drain region 116, and another high negative potential exists between the control gate 128 and the deep N-well 103 (the deep N-well 103 is grounded through a terminal), electrons stored in the floating gate 124 are affected by the electric field that transverses the tunnel oxide layer 122. The electrons thus transverse the tunnel oxide layer 122 by Fowler-Nordheim tunneling mechanism to com-

plete the Fowler-Nordheim erase.

[0031] Furthermore, when the present invention EEPROM device 100 performs reading, a third positive potential (such as +3.3V) is supplied to the source line electrically connected to the source region 114 of the P-type memory cell 106. Then a potential lower than the third positive potential (such as +1V) is supplied to the program bit-line. At this time, since a potential difference exists between the source line and the program bit-line, electrons stored in the floating gate 124 will flow out to cause a current measurable at the terminal of the source line. Oppositely, if there are no electrons stored in the floating gate 124, the current higher than a specific value cannot be measured at the terminal of the source line

[0032] The EEPROM device according to the present invention utilizes the P-type EEPROM cell to replace the prior art N-type EEPROM cell. Therefore, a P-type select gate transistor electrically connected to the program bit-line is utilized to perform the band-to-band tunneling induced hot-electrons program, and an N-type select gate transistor electrically connected to the erase bit-line is utilized to perform the Fowler-Nordheim tunneling erase. Since the band-to-band tunneling induced hot-electrons phe-

nomenon can generate a considerable current, the injection of hot electrons caused by band-to-band tunneling mechanism is faster than that caused by Fowler-Nordheim tunneling mechanism. Program speed and program efficiency are thus greatly improved to eliminate the need of the tunnel window utilized in the prior art EEPROM structure. When applying the present invention structure to a practical production line, byte-addressable EEPROM products having high programming speed, low operation voltage, high reliability, and small size are fabricated once the high gate coupling ratio and the high quality of the tunnel oxide are maintained.

[0033] Compared to the prior art EEPROM device and structure and method of operation, the present invention EEPROM device utilizes the P-type EEPROM cell to replace the N-type EEPROM cell. In addition, a P-type select gate transistor electrically connected to the program bit-line is utilized to perform the band-to-band tunneling induced hot-electrons program, and an N-type select gate transistor electrically connected to the erase bit-line is utilized to perform the Fowler-Nordheim tunneling erase. Due to the considerable current generated by the band-to-band tunneling induced hot-electrons phenomenon, the injec-

tion of hot electrons caused by band-to-band tunneling mechanism is faster than that caused by Fowler-Nordheim tunneling mechanism. Program speed is therefore greatly improved. Because of the obviously lifted program efficiency, the tunnel window, adapted in the prior art EEPROM device structure, can be replaced by a common tunnel oxide layer in the present invention EEPROM device structure. As a result, the problems of complex processing and raised cost incurred from misalignment, which usually occurs in the prior art, are avoided. The barrier to device shrinkage is not encountered. In addition, operation voltage is obviously lowered to expand the range of applicability under the industry stream of lightweight and small size.

[0034] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.